IN THE CLAIMS:

Please amend the claims as follows:

Claims 1-21 (Cancelled).

22. (Currently amended) A CMOS basic cell comprising:

an N-channel transistor, a P-channel transistor on a semiconductor substrate;

~~and an~~ at least one interconnect connected to said N-channel transistor or said P-channel transistor through ~~a~~ at least one contact hole ~~on a semiconductor substrate~~; and

an interconnect pattern which is ~~electrically~~ isolated from ~~said~~ every contact hole in said CMOS basic cell and ~~said~~ every interconnect in said CMOS basic cell,

~~and which~~ wherein said interconnect pattern exists between said N-channel transistor and said P-channel transistor, and

wherein said interconnect pattern is formed in an uppermost interconnect layer of said CMOS basic cell, and

wherein said CMOS basic cell has a boundary defining the edges of the CMOS basic cell, and at least one end of said interconnect pattern does not contact any edge of said CMOS basic cell.

23. (Currently amended) The CMOS basic cell of Claim 22, wherein said CMOS basic cell has a longitudinal axis, said interconnect pattern extending either ~~along a~~ perpendicular to said longitudinal axis ~~direction~~ or parallel to said longitudinal

axis ~~along a horizontal direction relative to a boundary between said N-channel transistor and said P-channel transistor~~.

24. (Currently amended) The CMOS basic cell of Claims 22 or 23 further comprising: a power supply pattern, a master pattern and another interconnect pattern different from said interconnect pattern,

wherein said another interconnect pattern exists between said N-channel transistor and said master pattern, said another interconnect pattern extending either ~~along a~~ perpendicular to ~~direction~~ or ~~along a horizontal~~ parallel ~~direction relative~~ to said longitudinal axis ~~a boundary between said N-channel transistor and P-channel transistor~~, said another interconnect pattern electrically disconnected from said N-channel transistor and said P-channel transistor and formed in said interconnect layer.

25. (Previously presented) The CMOS basis cell of any one of Claims 22 to 24, wherein said interconnect pattern is mutually connected electrically with an interconnect pattern of another CMOS basic cell, when said CMOS basic cell is adjacent to said another CMOS basic cell.

26. (Previously amended) The CMOS basic cell of any one of Claims 22 to 25, wherein two or more said CMOS basic cells are electrically connected by a higher interconnect pattern located in a layer that is higher than said interconnect pattern.

27. (Previously amended) The CMOS basic cell according to Claim 26, wherein said higher interconnect pattern is located in a region between said P-channel transistors and said N-channel transistors except the both ends of said interconnect

pattern, and

wherein said interconnect pattern which intersects said higher interconnect pattern is electrically connected with said higher interconnect pattern, said interconnect pattern being isolated from a second higher interconnect pattern which intersects said interconnect pattern.

28. (Previously presented) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to any one of Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit including a clock signal line by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

29. (Previously presented) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit including transistors connected to each other in parallel by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

30. (Previously presented) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a composite logic circuit by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

31. (Previously presented) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit including a control signal line by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

32. (Previously presented) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit for a memory by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

33. (Previously presented) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a flip-flop circuit having a scan test function by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

34. (Previously presented) A CMOS basic cell comprising:

an N-channel transistor and a P-channel transistor existing on a semiconductor substrate, said CMOS basic cell being electrical coupled with other adjacent CMOS basic cells;

wherein a gate of at least one of said N-channel transistor and said P-channel transistor has a hooked shape including a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in an opposite sideward direction at a lower portion thereof, and

a diffusion region of at least one of said N-channel transistor and said P-channel transistor having a hooked shape having a first bent part bending in one sideward

direction at an upper portion thereof and a second bent part bending in an opposite sideward direction at a lower portion thereof,

said upper portion of said gate is bent oppositely to said upper portion of said diffusion region.

35. (Previously presented) The CMOS basic cell of Claim 34, wherein a first N-channel transistor and a first P-channel transistor are formed to extend along a vertical direction, and

a second N-channel transistor is disposed on a side of said first N-channel transistor and a second P-channel transistor is disposed on a side of said first P-channel transistor, and

a gate of each of said first and second N-channel transistors and said first and second P-channel transistors is formed in the hooked shape.

36. (Previously presented) The CMOS basic cell of Claim 35, wherein the gates of said first and second N-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second bent part of the other gate when viewed along the vertical direction from one position in a horizontal direction, and

the gates of said first and second P-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second part of the other gate when viewed along the vertical direction from one position in the horizontal direction.

37. (Previously presented) The CMOS basic cell of Claim 35, wherein said first and second N-channel transistors share one diffusion region and said first and second

P-channel transistors share one diffusion region,

each of said diffusion regions is divided into a shared diffusion region shared by said first and second N-channel or P-channel transistors and positioned between the gates of said first and second N-channel or P-channel transistors; a first dedicated diffusion region positioned on a side of said gate of said first N-channel or P-channel transistor opposite to said shared diffusion region; and a second dedicated diffusion region positioned on a side of said gate of said second N-channel or P-channel transistor opposite to said shared diffusion region,

said first bent part is formed in said first dedicated diffusion region, and

said second bent part is formed in said second dedicated diffusion region.

38. (Previously presented) The CMOS basic cell according to any one of Claims 34 to 37, comprising, outside of a transistor region where said N-channel transistor are disposed, a fixed interconnect region where a power supply interconnect and a ground interconnect are disposed.

39. (Previously presented) The CMOS basic cell according to any one of Claims 34 to 37, said first bent part of said gate of said P-channel transistor and said first bent part of said diffusion region of said P-channel transistor of another CMOS basic cell is electrically connected with said higher interconnect pattern,

wherein said higher interconnect pattern extends along a horizontal direction to the perpendicular from said N-channel transistor to said P-channel transistor.

40. (Previously presented) A method for fabricating a gate array semiconductor

integrated circuit including a plurality of basic cells arranged in a horizontal direction, comprising a step of arranging a plurality of CMOS basic cells according to any one of Claims 34 to 37 in the horizontal direction in a manner that said first bent part of one CMOS basic cell overlaps said second bent part of another adjacent CMOS basic cell when viewed along a vertical direction from one position in a horizontal direction.

41. (Currently amended) A semiconductor integrated circuit including a plurality of CMOS basic cells arranged in the same direction,

wherein each CMOS basic cell is composed of first and second N-channel transistors and first and second P-channel transistors, and

a gate of [[of]] said first and second N-channel transistors and said first and second P-channel transistors of each cell is in a hooked shape having a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in the other sideward direction at a lower portion thereof,

wherein the gates of said first and second N-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second bent part of the other gate when viewed along an axis orthogonal to the axis extending parallel to the sideward directions in which ~~the~~ said first bent ~~portion~~ part and said second bent ~~portion~~ part extend, and

wherein the gates of said first and second P-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second bent part of the other gate when viewed along an axis orthogonal to an axis extending parallel to the

sideward directions in which ~~the~~ said first bent ~~portion~~ part and said second bent ~~portion~~ part extend.

42. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of CMOS basic cells;

each said CMOS basic cell comprising:

an interconnect layer formed in an uppermost layer of each of said plurality of CMOS basic cells, said interconnect layer comprising at least one interconnect operative for connecting signals to and from the corresponding CMOS basic cell;

an N-channel transistor and a P-channel transistor on a semiconductor substrate; and

an interconnect pattern which is capable of being electrically isolated from said N-channel transistor and said P-channel transistor and which is disposed between said N-channel transistor and said P-channel transistor,

wherein said interconnect pattern is formed in said uppermost layer of said CMOS basic cell,

wherein said interconnect pattern is only capable of being coupled to said N-channel transistor or said P-channel transistor by utilizing an interconnect pattern which is disposed in an interconnect layer located above said uppermost layer of said CMOS basic cell.

43. (Currently amended) The semiconductor integrated circuit of Claim 42,

wherein each said CMOS basic cell has a longitudinal axis, said interconnect pattern extending either ~~along a~~ perpendicular to said longitudinal axis ~~direction~~ or parallel to said longitudinal axis ~~along a horizontal direction relative to a boundary between said N-channel transistor and said P-channel transistor~~.

44. (Currently amended) The semiconductor integrated circuit of Claim 43, further comprising: a power supply pattern, a master pattern and another interconnect pattern different from said interconnect pattern,

wherein said another interconnect pattern exists between said N-channel transistor and said master pattern, said another interconnect pattern extending either ~~along a~~ perpendicular to ~~direction~~ or ~~along a horizontal~~ parallel ~~direction relative~~ to said longitudinal axis ~~a boundary between said N-channel transistor and P-channel transistor~~, said another interconnect pattern electrically disconnected from said N-channel transistor and said P-channel transistor and formed in said interconnect layer.

45. (Previously presented) The semiconductor integrated circuit of Claim 44, wherein said interconnect pattern is mutually connected electrically with an interconnect pattern of another CMOS basic cell, when said CMOS basic cell is adjacent to said another CMOS basic cell.

46. (Previously presented) The semiconductor integrated circuit Claim 45, wherein two or more said CMOS basic cells are electrically connected by a higher interconnect pattern located in a layer that is higher than said interconnect pattern.

47. (Cancelled)

48. (Cancelled)

49. (Cancelled)

50. (Cancelled)

51. (Cancelled)

52. (New) The CMOS basic cell of Claim 42, wherein said CMOS basic cell has a boundary defining the edges of the CMOS basic cell, and at least one end of said interconnect pattern does not contact any edge of said CMOS basic cell.

53. (New) A CMOS basic cell comprising:

an N-channel transistor and, a P-channel transistor on a semiconductor substrate;

an interconnect pattern which is disposed between said N-channel transistor and said P-channel transistor;

wherein said interconnect pattern is isolated from said N-channel transistor and said P-channel transistor;

wherein said interconnect pattern is formed in an uppermost interconnect layer of said CMOS basic cell, and

wherein said CMOS basic cell has a boundary defining the edges of the CMOS basic cell, and at least one end of said interconnect pattern does not contact any edge of said CMOS basic cell.

54. (New) The CMOS basic cell of Claim 53, wherein each said CMOS basic cell has a longitudinal axis, said interconnect pattern extending either perpendicular to

said longitudinal axis or parallel to said longitudinal axis.

55. (New) The CMOS basic cell of Claim 54, wherein said N-channel transistor and said P-channel transistor have a plurality of electrodes, and each electrode coupled to said N-channel transistor and said P-channel transistor is coupled to the uppermost layer of said CMOS basic cell via an interconnect.

56. (New) A CMOS basic cell comprising:

an N-channel transistor and, a P-channel transistor on a semiconductor substrate;

an interconnect pattern which is disposed between said N-channel transistor and said P-channel transistor;

wherein said interconnect pattern is isolated from said N-channel transistor and said P-channel transistor;

wherein said interconnect pattern is formed in an uppermost interconnect layer of said CMOS basic cell, and

wherein said N-channel transistor and said P-channel transistor have a plurality of electrodes, and each electrode coupled to said N-channel transistor and said P-channel transistor is coupled to the uppermost layer of said CMOS basic cell via an interconnect.

57. (New) The CMOS basic cell of claim 56, wherein said basic cell has a boundary defining the edges of the CMOS basic cell, and at least one end of said interconnect pattern does not contact any edge of said CMOS basic cell.

58. (New) The CMOS basic cell of Claim 53, wherein said interconnect pattern is only capable of being coupled to said N-channel transistor or said P-channel transistor by utilizing an interconnect pattern which is disposed in an interconnect layer located above said uppermost layer of said CMOS basic cell.

59. (New) The semiconductor integrated circuit of Claim 56, wherein said interconnect pattern is only capable of being coupled to said N-channel transistor or said P-channel transistor by utilizing an interconnect pattern which is disposed in an interconnect layer located above said uppermost layer of said CMOS basic cell.

60. (New) The CMOS basic cell of Claim 53, wherein said N-channel transistor and said P-channel transistor are isolated from each other by an insulating film on a semiconductor substrate.

61. (New) The CMOS basic cell of Claim 56, wherein said N-channel transistor and said P-channel transistor are isolated from each other by an insulating film on a semiconductor substrate.